CONTROLLED RESONANT HALF-BRIDGE INVERTER FOR POWER SUPPLIES AND ELECTRONIC BALLASTS

Field of the Invention

The present invention relates to the general subjects of power supplies and electronic ballasts for powering discharge lamps. More particularly, the present invention relates to a controlled resonant half-bridge inverter for use in power supplies and electronic ballasts.

Background of the Invention

Many power supplies and electronic ballasts for discharge lamps include an inverter and a resonant output circuit. Inverters are generally classified according to circuit topology (e.g., half-bridge, push-pull, etc.) and the approach used to control switching of the inverter transistors (e.g., self-oscillating or driven). Inverters that drive a resonant output circuit are sometimes referred to as resonant inverters.

In a number of applications, such as electronic ballasts for gas discharge lamps, driven inverters have come to be preferred over self-oscillating inverters. Although each type of inverter has its advantages, it is generally acknowledged that driven inverters are easier to design and to control. In particular, driven inverters are preferred for ballasts that provide variable illumination (dimming) and/or that include circuitry for protecting the ballast under various fault conditions.

It is known that energy efficiency is optimized when the inverter is operated at the "effective" resonant frequency of the output circuit. The effective resonant frequency varies as the load on the output circuit varies. For example, when the output circuit is unloaded (e.g., with the lamp(s) removed or inoperative), the effective resonant frequency is simply the natural resonant frequency of the output circuit. When the output circuit is fully loaded (e.g., with the lamp(s) operating at rated power), the effective resonant frequency (e.g., 44.5 kilohertz) is significantly lower than the natural resonant frequency (e.g., 48 kilohertz).

Typically, driven resonant inverters are designed so that the switching frequency is set at a value (e.g., 50 kHz) that is somewhat higher than the natural resonant frequency (e.g., 48 kHz). Because of potentially wide variations in the load and in the DC voltage that powers the inverter, this margin is necessary in order to ensure that the switching frequency remains higher than the effective resonant frequency under all loading conditions. Without this margin, the switching frequency may actually end up being less than the effective resonant frequency under certain loading conditions, in which case highly dissipative "hard switching" of the inverter transistors will occur. However, as this margin ensures that the switching frequency will not be equal to the effective resonant frequency, it has the undesirable effect of producing less than optimal inverter efficiency (because, as previously mentioned, inverter efficiency is optimized when the switching frequency is equal to the effective resonant frequency).

What is needed, therefore, is a driven resonant inverter in which the switching frequency automatically tracks the effective resonant frequency under loaded conditions. Such an inverter would provide improved efficiency and would thus represent a significant advance over the prior art.

Brief Description of the Drawings

FIG. 1 is a partial block-diagram electrical schematic of a controlled resonant half-bridge inverter, in accordance with a preferred embodiment of the present invention.

FIG. 2 is a detailed electrical schematic of a controlled resonant half-bridge inverter, in accordance with a preferred embodiment of the present invention.

FIG. 3 describes several voltages associated with the operation of the circuit illustrated in FIG. 2, when the upper inverter transistor is operated at an approximately 50% duty cycle, in accordance with a preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

In a preferred embodiment of the present invention, as described in Figure 1, a circuit 10 includes a driven half-bridge type inverter 100, a resonant output circuit 300, and a control circuit 400,500.

Inverter 100 has an upper transistor 120, a lower transistor 130, and a driver circuit 200 for commutating transistors 120,130 in a substantially complementary manner (i.e., when transistor 120 is on, transistor 130 is off, and vice versa). Resonant output circuit 300 is coupled between inverter 100 and a load. In a preferred application of circuit 10, the load consists of one or more gas discharge lamps 20,30.

Control circuit 400,500 is coupled between resonant output circuit 300 and driver circuit 200 of inverter 100. During operation, control circuit 400,500 monitors a signal within resonant output circuit 300. In response to the signal reaching a predetermined level, control circuit 400,500 directs driver circuit 200 to render upper transistor 120 conductive and lower transistor 130 non-conductive for a predetermined first period. The first period is described as "predetermined" because it is set internally within the control circuit. Upon completion of the first period, control circuit 400,500 directs driver circuit 200 to render upper transistor 120 non-conductive and lower transistor 130 conductive for a second period until such time as the signal within resonant output circuit 300 again reaches the predetermined level. In this way, control circuit 400,500 synchronizes the switching of inverter transistors 120,130 based upon the phase of the signal within resonant output circuit 300. More particularly, control circuit 400,500 ensures that the turn-on of upper transistor 120 and the turn-off of lower transistor 130 are controlled by the phase of the signal within resonant output circuit 300, thus providing an arrangement wherein the switching frequency is automatically adjusted so as to track the effective resonant frequency of output circuit 300. It is believed that these attributes of circuit 10 provide enhanced energy efficiency by reducing the power dissipation in inverter transistors 120,130.

As described in Figure 1, control circuit 400,500 preferably comprises a phase detector circuit 400 and a one-shot circuit 500.

Phase detector circuit 400 has a detector input 402 and a detector output 404, the latter being coupled to resonant output circuit 300. During operation, phase detector circuit 400 generates a trigger signal at detector output 404 when the monitored signal within resonant output circuit 300 reaches the predetermined level. Preferably, phase detector circuit 400 generates the trigger signal by causing the voltage at detector output 404 to fall below a predetermined trigger threshold for a limited period of time that is substantially less than the first period. After the limited period of time, the voltage at detector output 404 recovers and exceeds the predetermined trigger threshold.

One-shot circuit 500 is coupled between detector output 404 and driver circuit 200. During operation, when phase detector circuit 400 provides the trigger signal, one-shot circuit 500 directs driver circuit 200 to render upper transistor 120 conductive and lower transistor 130 non-conductive for the first period. The first period is set internally within one-shot circuit 500. Preferably, one-shot circuit 500 includes a control output 502 that is coupled to driver circuit 200. During operation, when phase detector circuit 400 provides the trigger signal, one-shot circuit 500 generates a control voltage at control output 502. The control voltage has a duration that is approximately equal to the first period.

Preferred detailed structures for inverter 100, output circuit 300, phase detector circuit 400, and one-shot circuit 500 are now described with reference to Figure 2, as follows.

Inverter 100 includes first and second input terminals 102,104, an inverter output terminal 106, an upper transistor 120, a lower transistor 130, and a driver circuit 200. Input terminals 102,104 receive a source of substantially direct current (DC) voltage, V_{DC}. V_{DC} may be provided by any of a number of arrangements known to those skilled in the art; one such arrangement consists essentially of a full-wave rectifier (coupled to a source of conventional 60 hertz alternating current) followed by a boost converter. Second input terminal 104 is

coupled to circuit ground 60. Upper transistor 120 is coupled between first input terminal 102 and inverter output terminal 106; more specifically, upper transistor 120 has a drain 124 coupled to first input terminal 102, a source 126 coupled to output terminal 106, and a gate 122 coupled to driver circuit 200. Lower transistor 130 is coupled between inverter output terminal 106 and circuit ground 60; more specifically, lower transistor 130 has a drain 134 coupled to output terminal 106, a source 136 coupled to circuit ground 60, and a gate 132 coupled to driver circuit 200.

Driver circuit 200 has a control input 202 that is coupled to one-shot circuit 500, and a plurality of outputs 204,206,208 that are coupled to inverter transistors 120,130. Preferably, driver circuit 200 is implemented using a commercially available integrated circuit 210, such as the IR2104 high-side driver integrated circuit manufactured by International Rectifier, along with associated peripheral components 220,222,230,240,250,260. As the operation of peripheral components 220,222,230,240,250,260 is explained in application notes and data books pertaining to the IR2104 IC, it is known to those skilled in the art and will not be described in further detail herein. The DC supply voltage, which is depicted as "+12 V" in Figure 2, may be provided by any of a number of circuits that are well known to those skilled in the art. For example, in those applications where V_{DC} is supplied by a combination of a full-wave rectifier and a boost converter, the DC supply voltage may be derived from the same circuitry that provides operating power to the control circuit for the boost converter.

As shown in Figure 2, control input 202 of driver circuit 200 is coupled to the "IN" input 212 of integrated circuit 210. During operation, control input 202 receives a control voltage V_0 from one-shot circuit 500 that varies between a low level (e.g., 0 volts) and a high level (e.g., +12 volts). In response to the control voltage being at the high level, integrated circuit 210 provides a high level voltage (e.g., 12 volts) between terminals 204,206 (i.e., V_1) and a low level voltage (e.g., 0 volts) between terminal 208 and circuit ground 60 (i.e., V_2), thereby causing upper transistor 120 to be on and lower transistor 130 to be off. Conversely, when the control voltage is at the low level, integrated circuit 210 sets V_1 low and V_2 high, thereby causing to causing upper transistor 120 to be

off and lower transistor 130 to be on. In this way, the control voltage V_0 provided to integrated circuit 210 by one-shot circuit 500 controls the commutation of inverter transistors 120,130.

Referring again to Figure 2, resonant output circuit 300 comprises first and second output connections 302,304, a resonant inductor 310, a resonant capacitor 320, a direct current (DC) blocking capacitor 330, and a startup resistor 340. Output connections 302,304 are adapted for connection to a load, such as one or more gas discharge lamps 20,30. Resonant inductor 310 is coupled between inverter output terminal 106 and first output connection 302. Resonant capacitor 320 is coupled between first output connection 302 and circuit ground 60. DC blocking capacitor 330 is coupled between second output connection 304 and circuit ground 60. Startup resistor 340 is coupled between first input terminal 102 of inverter 100 and first output connection 302.

During operation, resonant capacitor 320 has a substantially sinusoidal voltage, Vx. Preferably, Vx is the signal that is monitored by phase detector circuit 400, in which case the detector input 402 of phase detector circuit 400 is coupled to first output connection 302. Preferably, phase detector circuit 400 generates the trigger signal when Vx reaches its maximum negative level, or at least within a very short period of time thereafter. When V_X is at its maximum negative level, the current flowing through resonant inductor 310 is approximately zero. Thus, upper transistor 120 will be turned on under a substantially zero current condition, which minimizes the switching stress and turn-on switching losses in upper transistor 120.

The basic operation of resonant output circuit 300 is well understood by those skilled in the art and thus will not be further elaborated upon herein. However, the function of startup resistor 340 merits brief description. Startup resistor 340 charges resonant capacitor 320 prior to inverter startup so that, once the inverter starts and lower transistor 130 turns on, current will flow in the resonant circuit. This causes Vx to be sinusoidal (in a transient manner) and thus allows phase detector circuit 400 and one-shot circuit 500 to subsequently turn on upper transistor 120 for the first time. Once upper transistor 120 is turned on for the first time, the resonant circuit receives a substantial amount of

energy from the DC source (V_{DC}), at which point the presence of startup resistor 340 is largely immaterial to the operation of circuit 10.

Preferred structures for phase detector circuit 400 and one-shot circuit 500 are now described with reference to Figure 2.

Phase detector circuit 400 comprises a detector input 402, a detector output 404, a transistor 430, a first capacitor 410, a diode 412, a first resistor 420, a second resistor 440, a second capacitor 460, and a third resistor 450. Transistor 430 is preferably implemented as a NPN-type bipolar junction transistor having a base 432, a collector 436, and an emitter 434. Emitter 434 is coupled to circuit ground 60. First capacitor 410 is coupled between detector input 402 and base 432 of transistor 430. Diode 412 has a cathode 416 coupled to base 432 and an anode 414 coupled to circuit ground 60. First resistor 420 is coupled between base 432 and circuit ground 60. Second resistor 440 is coupled between detector output 404 and a direct current (DC) supply voltage (e.g., +12 volts). Second capacitor 460 and third resistor 450 are each coupled between detector output 404 and collector 436 of transistor 430.

During operation of phase detector circuit 400, capacitor 410 and resistor 420 function as a positive-going slope detector. More specifically, once V_X reaches its maximum negative level, the slope of V_X begins to go positive and increases with V_X. Consequently, an increasing positive current flows into detector input 402 and through capacitor 410 and resistor 420. When the positive current through resistor 420 reaches a certain level, the voltage across resistor 420 becomes high enough (e.g., 0.6 volts) to turn on transistor 430. Transistor 430 will remain on for about as long as the slope of V_X remains sufficiently positive to provide enough current to keep the voltage across resistor 420 from falling below about 0.6 volts.

Referring momentarily to Figure 3, when transistor 430 is first turned on at $t=t_1$, the voltage V_T at detector output 404 is pulled down from +12 volts to zero. As transistor 430 remains on ($t_1 < t < t_3$), V_T begins to recover and increases at a rate governed by the values of resistors 440,450 and capacitor 460. Eventually, capacitor 460 peak charges and V_T levels off at a certain value (e.g.,

8 volts) as determined by the relative values of resistors 440,450. The brief period of time ($t_1 < t < t_2$) during which V_T is between zero and 4 volts corresponds to the trigger signal that controls the operation of one-shot circuit 500.

Turning back to Figure 2, one-shot circuit 500 is preferably implemented as a 555 type timer circuit that is operated in a "monostable" mode; that is, the timer circuit is configured to provide an output voltage that goes high when a suitable momentary trigger voltage is provided, remains high for a predetermined period of time (i.e., the first period), then goes low and remains low for a period of time (i.e., the second period) until the timer is re-triggered. More specifically, in a preferred embodiment, one-shot circuit 500 includes a timer integrated circuit 510 and a timing network 530,532,540. Timer integrated circuit 510, which is preferably realized by a MC1455 integrated circuit manufactured by Motorola, is operated in a monostable mode and has a trigger input 512 (i.e., pin 2), an output 514 (i.e., pin 3), and a timing input 516 (i.e., pin 6). Trigger input 512 is coupled to detector output 404 of phase detector circuit 400. Output 514 is coupled to driver circuit 200 via resistor 520, control output 502 and control input 202. Timing network 530,532,540, which determines the first period, includes a timing resistance 530,532 and a timing capacitance 540. Timing resistance 530,532 is coupled between the DC supply voltage ("+12 V" in Figure 2) and timing input 516 of timer integrated circuit 510. Timing capacitance 540 is coupled between timing input 516 and circuit ground 60.

During operation of one-shot circuit 500, in the absence of a trigger signal at pin 2 of timer IC 510, the voltage at pin 3 (and, correspondingly, the voltage V_0 at control output 502) will be low (e.g., zero). That is, when V_T is greater than about +4 volts (corresponding to one-third the DC supply voltage), V_0 remains at zero. Conversely, when V_T falls below +4 volts, timer IC 510 treats that as a trigger signal and causes V_0 to go high (e.g., 12 volts). Once triggered, V_0 will remain at 12 volts for the first period, as set by timing network 530,532,540. Upon expiration of the first period, provided that a trigger signal is not present (i.e., $V_T > 4$ volts), V_0 will revert back to zero and remain at zero until such time as a new trigger signal (i.e., $V_T < 4$ volts) is provided.

Preferably, timing resistance 530,532 is adjustable; thus, in Fig. 2, resistor 532 is depicted as a variable resistor. The first period may be varied via adjustment of resistor 532. More specifically, an increase in the timing resistance increases the first period and increases the amount of power that is processed by inverter 100 and output circuit 300; conversely, a decrease in the timing resistance decreases the first period and thus reduces the amount of power that is processed by inverter 100 and output circuit 300. Although it is possible to adjust the first period so that the duty cycle of upper transistor 120 is very low (e.g., 10% or lower), in practice it is recommended that the duty cycle of the upper transistor be set at no less than about 30%. In a prototype circuit configured substantially as described herein, it was observed that operation with a duty cycle of less than about 30% for upper transistor 120 produced undesirable hard switching in lower transistor 130.

As a design matter, the timing resistor 532 should be set so that the first period is less than one-half of the period corresponding to the highest effective resonant frequency that will be encountered during operation. For example, if the highest effective resonant frequency that will be encountered during operation is 50 kilohertz (period = 1/50,000 = 20 microseconds), then timing resistor 532 should be set to provide a first period that is less than 10 microseconds. As a consequence of satisfying this design constraint for the first period, the duty cycle of upper transistor 120 will be less than 50% during operation.

Although depicted in Figure 2 as a series combination of a fixed resistor 530 and a variable resistor 532, it should be appreciated that the timing resistance may be realized by any of a number of alternative circuits known to those skilled in the art. For example, variable resistor 532 may be replaced by a circuit that injects an adjustable amount of current into pin 6 of timer IC 510 so as to reduce the first period and, consequently, reduce the amount of power provided to the load.

The detailed operation of circuit 10 is now explained with reference to Figures 2 and 3 as follows.

Figure 3 gives approximate plots of several voltages that occur during steady-state operation of the circuit of Figure 2. More specifically: V_X is the voltage across resonant capacitor 320; V_T is the trigger voltage provided at detection output 404 of phase detector circuit 400; V_0 is the control voltage provided at the control output 502 of one-shot circuit 500 and the control input 202 of driver circuit 200; V_1 is the gate-to-source voltage for upper inverter transistor 120; V_2 is the gate-to-source voltage for lower inverter transistor 130; V_{INV} is the inverter output voltage provided at inverter output terminal 106.

Figure 3 describes the aforementioned voltages when timing network 530,532,540 is set so as to provide an approximately 50% duty cycle for upper transistor 120; that is, Figure 3 corresponds to a situation where resistor 532 is set at its maximum value (e.g., 10 kilohms). Resistor 532 may be reduced from its maximum value so as to provide a duty cycle of less than 50% for upper transistor 120, in which case the duty cycle of lower transistor 130 will increase correspondingly. As previously mentioned, it is important that the first period be set such that it does not exceed one-half of the period corresponding to the highest effective resonant frequency that will be encountered during operation, in which case the duty cycle of upper transistor 120 will be somewhat less than 50%.

Referring to Figures 2 and 3, prior to $t=t_1$, V_T is at its initial value of 12 volts, V_0 and V_1 are low (i.e., zero), and V_2 is high (i.e., 12 volts). Correspondingly, upper transistor 120 is off, lower transistor 130 is on, and the inverter output voltage V_{INV} is at zero. During the period $t < t_1$, the slope of V_X is negative, so phase detector circuit 400 is prevented from providing a trigger pulse. More specifically, while the slope of V_X is negative, only negative current can flow into detector input 402 (i.e., a positive current flows up from circuit ground 60, through diode 412, through capacitor 410, and out of detector input 402), so transistor 430 remains off due to the presence of a negative voltage between base 432 and emitter 434.

At $t=t_1$, V_X reaches its negative peak value and its slope begins to go positive. Consequently, within a very short time after t_1, positive current begins to flow into detector input 402 and through capacitor 410 and resistor 420. Once the positive current reaches a sufficient value (i.e., 600 microamperes or so), the voltage across resistor 420 becomes large enough (i.e., 0.6 volts or so) to turn on transistor 430. With transistor 430 turned on, V_T rapidly drops from its initial value of 12 volts to zero. Due to scale limitations, the transition in V_T is shown as occurring at $t=t_1$, but it should be understood that in reality the transition occurs shortly after $t=t_1$. In response to V_T falling below the trigger threshold of 4 volts, the voltage V_0 at the output 514 of timer IC 510 goes high (i.e., 12 volts). Correspondingly, with V_0 at 12 volts, the voltage V_2 provided between the LO output (218) of driver IC 210 and circuit ground 60 goes low (e.g., 0 volts) and lower transistor 130 turns off. At about the same time, the voltage V_1 provided between the HO (214) and VS (216) outputs of driver IC 210 goes high (e.g., 12 volts) and turns on upper transistor 120. Consequently, the inverter output voltage V_{INV} goes from zero to $+V_{DC}$.

Once triggered by V_T falling below 4 volts, V_0 remains high for the duration of the first period (i.e., $t_1 < t < t_3$) as dictated by the values of resistors 520,530 and capacitor 540.

During the time $t_1 < t < t_2$, with transistor 430 turned on, capacitor 460 (which was initially uncharged prior to the turn on of transistor 430) is coupled to circuit ground 60 and begins to charge up from the +12 volt DC supply via resistor 440. Consequently, V_T rises at a rate governed by the capacitance of capacitor 460 and the resistances of resistors 440,450. At $t=t_2$, V_T reaches the threshold value of 4 volts, at which point the trigger pulse is no longer supplied to one-shot circuit 500. As a design matter, it is essential to ensure that the duration of the trigger pulse ($t_1 < t < t_2$) is less than the smallest desired value for the first period ($t_1 < t < t_3$). Stated another way, it is essential that V_T exceed 4 volts (at $t=t_2$) well before the end of the first period (at $t=t_3$). This is required so that, by the time that the first period reaches its end at $t=t_3$, the trigger pulse (i.e., $V_T < 4$ volts) is no longer present and one-shot circuit 500 is thus prevented

from operating in an undesirable manner (i.e., turning the upper transistor 120 off for a brief instant but then almost immediately back on again).

After $t=t_2$, capacitor 460 continues to charge up and V_T correspondingly increases until capacitor 460 becomes peak charged (to a voltage determined by the ratio of resistors 440,450), at which point V_T reaches its peak value of about 8 volts. V_T then remains at about 8 volts for as long as transistor 430 remains on. Transistor 430 remains on for as long as the slope of V_X is sufficiently positive to supply enough current to maintain about 0.6 volts across resistor 420.

Shortly before $t=t_3$, the slope of V_X becomes sufficiently small such that the current flowing into detector input 402 becomes insufficient (e.g., less than 600 microamperes) to keep transistor 430 on. Thus, transistor 430 turns off shortly before $t=t_3$; again, due to scale limitations, this is depicted in Figure 3 as occurring substantially simultaneously with $t=t_3$, although in reality it occurs shortly before $t=t_3$. With transistor 430 off, V_T rises to 12 volts and capacitor 460 discharges through resistor 460. V_T remains at 12 volts until V_X once again reaches its negative peak value (at $t=t_4$).

Recall that, at $t=t_1$, one-shot circuit 500 was triggered and V_0 went from zero to 12 volts, causing V_1 to go high (turning on upper transistor 120) and V_2 to go low (turning off lower transistor 130). V_0 remains high until expiration of the first period, as determined by timing network 530,532,540, at t=t3.

At $t=t_3$, the first period expires and V_0 goes low. Consequently, V_1 goes low (turning off upper transistor 120) and V_2 goes high (turning on lower transistor 130). Correspondingly, V_{INV} drops from $+V_{DC}$ to zero. V_0, V_1, V_2, and V_{INV} then remain at these values until such time as V_X once again reaches it negative peak value at t=t4, at which point the aforementioned events are repeated.

Preferred components for implementing inverter 100, driver circuit 200, output circuit 300, phase detector circuit 400, and one-shot circuit 500 are described as follows:

Inverter 100:

Transistors 120,130: IRFBC40

Driver circuit 200:

Driver IC 210: IR2104 (International Rectifier)

Resistors 220, 222: 33 ohms

Resistor 230: 1 kilohms

Capacitor 240: 0.47 microfarad

Diode 250: 1N4937

Capacitor 260: 0.1 microfarad

Output circuit 300:

Resonant inductor 310: 2.8 millihenry

Resonant capacitor 320: 3.9 nanofarad

DC blocking capacitor 330: 0.1 microfarad

Startup resistor 340: 1 megohm

Phase detector circuit 400:

Capacitor 410: 220 picofarad

Diode 412: 1N4148

Resistor 420: 1 kilohm

Transistor 430: 2N3904

Resistor 440: 10 kilohm

Resistor 450: 22 kilohm

Capacitor 450: 220 picofarad

One-shot circuit 510:

Timer IC 510: MC1455 (Motorola)

Resistor 520: 10 kilohm

Resistor 530: 1 kilohm

Resistor 532: 0 – 10 kilohm (variable)

Capacitor 540: 0.001 microfarad

Capacitor 550: 0.01 microfarad

In a prototype ballast configured substantially as described herein for powering a 50 watt lamp load, the input power was measured at about 53 watts (versus about 55 watts for a comparable prior art ballast). Thus, circuit 10 is significantly more efficient than comparable prior art circuits.

It is believed that an additional benefit of circuit 10 is that, in the unlikely event of a short circuit across output connections 302,304, inverter switching will cease within one high frequency cycle following occurrence of the short circuit.

Although the present invention has been described with reference to certain preferred embodiments, numerous modifications and variations can be made by those skilled in the art without departing from the novel spirit and scope of this invention.

What is claimed is: